MOCVD SELECTIVE DEPOSITION OF C-AXIS ORIENTED $Pb_5Ge_3O_{11}$ THIN FILMS ON HIGH-K GATE OXIDES

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Field of the Invention

This invention relates to ferroelectric thin film processes, ferroelectric memory device structures and integrated processes for ferroelectric non-volatile memory devices, and specifically to a method of forming a c-axis oriented PGO thin film on a high-k oxide.

Background of the Invention

Metal, ferroelectric, insulator, and silicon (MFIS) transistor ferroelectric memory devices have been proposed, and c-axis oriented $Pb_5Ge_3O_{11}$ (PGO) thin films exhibit good ferroelectric and electrical properties for one transistor (1T) memory device applications. Extremely high c-axis oriented PGO thin films can be deposited on high-k gate oxides, and working 1T-memory devices with PGO MFIS memory cells have been fabricated. However, the integration process induces damage, such as etching damage, reduces properties of ferroelectric RAM (FRAM) devices, and results in high surface roughness making alignment difficult. In order to resolve these problems, selective deposition processes have been developed to simplify integration processes and improve the properties of MFIS transistor ferroelectric memory devices.

The formation of seed layers for MOCVD of ferroelectric films is described in U. S. Patent Application Serial No. 10/020,868, filed May 8, 2001, by Li *et al.*, for *Seed layer processes for MOCVD ferroelectric thin films deposited on high-k gate oxides*.

Summary of the Invention

A method of forming a PGO thin film on a high-k dielectric includes preparing a silicon substrate, including forming a high-k gate oxide layer thereon; patterning the high-k gate oxide; annealing the substrate in a first annealing step; placing the substrate in a MOCVD chamber; depositing a PGO thin film by injecting a PGO precursor into the MOCVD chamber; and annealing the structure having a PGO thin film on a high-k gate oxide in a second annealing step.

It is an object of the invention to provide a selective deposition method for c-axis PGO thin films on high-k gate oxides, including ZrO_X (X=0-2), HfO_X (X=0-2), TiO_2, Al_2O_3, La_2O_3, and mixtures thereof.

Another object of the invention is to provide for a simplified integration process for c-axis PGO thin films.

A further object of the invention is to provide a PGO MFIS transistor having improved electrical characteristics.

This summary and objectives of the invention are provided to enable quick comprehension of the nature of the invention. A more thorough understanding of the invention may be obtained by reference to the following detailed description of the preferred embodiment of the invention in connection with the drawings.

Brief Description of the Drawings

Fig. 1 depicts an x-ray pattern of PGO thin film deposited on a HfO_2 gate oxide of a test wafer by the method of the invention.

Fig. 2 depicts an x-ray pattern of PGO thin film which has been selectively deposited on a patterned HfO_X device wafer.

Fig. 3 depicts a microphotograph of selective deposition of a first PGO thin film deposited on HfO_2.

Fig. 4 depicts a microphotographs of selective deposition of a second PGO thin film deposited on HfO_2.

Detailed Description of the Preferred Embodiments

The method of the invention provides for selective deposition of c-axis $Pb_5Ge_3O_{11}$ (PGO) thin films on high-k gate oxides, including ZrO_X (X=0-2), HfO_X (X=0-2), TiO_2, Al_2O_3, La_2O_3, and mixtures thereof, to simplify the integration processes and improve the properties of PGO MFIS transistor ferroelectric memory devices.

The method of the invention provides for selective growth of ferroelectric PGO thin films on high-k gate oxides for metal, ferroelectrics, insulator, and silicon (MFIS) memory device fabrication. Using the method of the invention, there is no need to etch the ferroelectric material. As a result, etching-induced damage to the ferroelectric layer is avoided. Because of the selective deposition of PGO on patterned high-k gate oxide, other than on a field oxide, the alignment problem is also resolved.

P-type silicon wafers are used as the substrate for a PGO MFIS device. The method of the invention includes providing a silicon wafer, preferably Si (100) wafers, having a SiO_2 film deposited thereon. A gate oxide, of high-k material, such as a layer of Hf or HfO_2/Hf, having a thickness of between about 3.5 nm to 10 nm, is deposited on the SiO_2 film. The Hf or HfO_2/Hf film is patterned using chemical mechanical polishing (CMP), or etching. The structure is annealed in a first annealing step in forming gas at between about 400°C to 450°C for between about ONE minutes to 40 minutes.

An oxide metal organic chemical vapor deposition (MOCVD) chamber is used for the selective deposition of c-axis oriented $Pb_5Ge_3O_{11}$ thin films on the high-k gate oxide, wherein the structure is masked to prevent deposition of PGO on any exposed SiO_2. The structure is again annealed in a second annealing step at a temperature of between about 500°C to 560°C, for a time of between five minutes to thirty minutes.

The selective MOCVD processes includes preparing $[Pb(thd)_2]$ and $[Ge(ETO)_4]$ in a molar ratio of between about 5 to 5.5:3, which are dissolved in a mixed solvent of butyl ether or tetrahydrofuran, isopropanol and tetraglyme in a molar ratio of about 8:2:1. THD is $C_{11}H_{19}O_2$ and ETO is OC_2H_5. The precursor solutions has a concentration of 0.1 mole/liter of PGO. The solution is injected into a vaporizer at temperature in the range of between about 150°C to 240°C by a pump at a rate of 0.02 ml/min to 0.2 ml/min to form a precursor gas. The feed line was maintained at a temperature of between about 150°C to 245°C. Two precesses may be used to form the PGO thin film on the high-k dielectric material:

Process 1: a substrate of Hf/HfO_2 or Hf is prepared prior to deposition of PGO. MOCVD chamber parameters are maintained during the deposition process, which parameters include, in this embodiment of the method of the invention, a deposition temperature of between about 500°C to 560°C and a deposition pressure of between about one torr. to ten torr. is maintained in the deposition chamber. The chamber has an oxygen partial pressure of between about 30% to 50%, a vaporizer temperature of between about 180°C to 200°C, a vaporizer pressure of between about 30 torr. to 50 torr., and a precursor solution delivery rate of between about 0.02 ml/min to 0.2 ml/min, which is maintained for a deposition time of between about one hour to three hours, depending on desired film thickness. The structure is annealed in the second annealing step at a temperature in a

range of between about 500°C to 560°C for between about five minutes to 30 minutes in an oxygen atmosphere. This results in a PGO thin film having a thickness of between about 50 nm to 1000 nm.

Process 2: A two step deposition processes is used for this embodiment of the method of the invention. In the first step, a selective seed layer of PGO is deposited on a Hf or HfO_x (x=0-2)/Hf layer, at a deposition temperature of between about 500°C to 560°C at a pressure of between about 1 torr. to 10 torr, in an atmosphere having an oxygen partial pressure of between about 20% to 50%. The vaporizer temperature is between about 180°C to 200 °C and the pressure is between about 30 torr. to 50 torr. The precursor solution delivery rate is between about 0.02 ml/min to 0.1 ml/min, and the deposition time is in a range of between about five minutes to twenty minutes. This results in a PGO thin film having a thickness of between about 10 nm to 30 nm.

The second step of the deposition process includes selective deposition of PGO on the PGO seed layer formed in the first step of this process, wherein the deposition temperatures is between about 380°C to 420°C and the chamber pressure is between about five torr. and ten torr. The chamber is maintained at an oxygen partial pressure of between about 30% to 40%, at a vaporizer temperature of between about 200°C to 240°C, and a solution delivery rate of between about 0.1 ml/min to 0.2 ml/min, for a deposition time of between about one hour to three hours, depending on the desired film thickness. The structure is annealed in the second annealing step in an oxygen atmosphere at a temperature in a range of between about 500°C to 560°C for between about five minutes to 30 minutes. This results in a PGO thin film having a thickness of between about 50 nm to 1000 nm.

The Experimental Results

The phases of the films were identified using x-ray diffraction. The microstructures are measured by microscope.

Fig. 1 depicts the x-ray pattern of PGO thin film deposited on an HfO_2 gate oxide of a test wafer, and demonstrates that an extremely high c-axis oriented PGO thin film is present. Fig. 2 depicts the x-ray pattern of PGO thin film that was selectively deposited on patterned HfO_X (x=0-2) device wafers, and confirms that the selectively deposited thin film on the patterned HfO_X (x=0-2) device wafer is c-axis oriented PGO thin film.

Figs. 3 and 4 depict microphotographs of selective deposition of PGO thin films on HfO_2. These figures confirm that PGO thin films have been selectively deposited on HfO_X (x=0-2) gate oxide, other than on SiO_2.

Thus, a method for MOCVD selective deposition of c-axis oriented $Pb_5Ge_3O_{11}$ thin films on high-k gate oxides has been disclosed. The method of the invention is significant in that no etching of the PGO thin film is required. It will be appreciated that further variations and modifications thereof may be made within the scope of the invention as defined in the appended claims.